C U R R I C U L U M V I T A E

F A T E M E H K A S H F I

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Education

Aug 2008- now	**PhD student in Electrical Engineering,** *University of Southern California, Electrical Engineering Department.* Advisor: Prof. Pedram
Sep 2005 - Feb 2008	**M.Sc. in Electronics, Circuit and Systems,** *School of Electrical and Computer Engineering, University of Tehran*, Tehran- Iran. **Master Thesis Title:** Design of High Speed and Low Power Digital Computational Circuits in Sub 70nm Technologies
Sep 2001- Sep 2005	**B.Sc. in Electrical Engineering (Electronics)**, *School of Electrical and Computer Engineering, University of Tehran*, Tehran- Iran.
Sep 1997 – Sep 2001	**Diploma**, *Farzanegan High School*, under the supervision of NODET (National Organization for Developing Exceptional Talents), Tehran-Iran.

Research Interests

- Statistical timing analysis and optimization
- Low power digital integrated circuit design
- Computational digital circuits and memory design

Publications

Journal Papers

- **F. Kashfi**, S. Mehdi Fakhraie, and S.Safari "Designing an ultra-high-speed multiply-accumulate structure," *Microelectronics Journal*, Vol. 39, No. 12, pp. 1476-1484, Dec 2008,
- **F. Kashfi**, A. Agah, S. Mehdi Fakhraie, and S.Safari "15GHz Carrylook-Ahead Low-Voltage-Swing Adder," *Journal of IEICE Electronics Express*, vol. 4, no. 22, pp 696-700, (2007)

Conference Papers

- **F. Kashfi**, S. Mehdi Fakhraie, and S.Safari "A 65nm 10GHz pipelined MAC Structure," accepted in *IEEE ISCAS'08,* pp-460-463, May 2008.

- **F. Kashfi**, and N. Masoumi, "Optimization of speed and power in a 16-bit carry skip adder in 70nm technology," in proc. *IEEE MWSCAS'06,* vol.1, pp. 28-31, Porto Rico, Aug. 2006.
- **F. Kashfi**, and S. Mehdi Fakhraie, "Implimentation of a high-speed low-power 32-bit adder in 70nm technology," in proc. *IEEE ISCAS'06,* pp. 4-9, Greece, May 2006.

Honors

- Viterbi School Dean's Doctoral Fellowships Award, University of Southern California 2008-2009

Graduate Course Works

- VLSI System Design (A and B)
- Computer Aided Design
- Analysis of Algorithms
- Bioinspired Computing
- Low Power Integrated Circuit Design
- Analog Integrated Circuit Design
- Data Converters and Analog Filters
- Fabrication of Electronic Components
- Custom Design of DSP Systems

Presentations

- Attending and Lecture Presentation in IEEE ISCAS 2006 conference held in Greece in May 2006.

Work Experience

Jan. 2006- Feb 2007 — Working in *Sina Microelectronics* Inc as analog design engineer. Designing a PCI based Linecard board with 4 FXSs and 2 FXOs for IP PBX application. The design also included manual place and route; CPLD programming, synthesis and implementation; and driver design.

Computer and English Skills

- **Programming Language**: Pascal, C/C++, Delphi,
- **CAD Tools**: ALTERA's MAXplus II, ModelSim, Verilog, Quartus.
- **Software Packages:** In depth practical experience with Application Packages such as: Cadence, Synopsys, Nanosim, MATLAB, ADS.
- **TOEFL** (*Internet Based Test* held on Oct 6th 2007) Total Score: **105/120**
  - Reading: **26/30** Listening: **28/30** Speaking: **23/30** Writing: **28/30**