Arash Fayyazi

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EDUCATION

Ph.D. in Electrical Engineering, Minor- Computer Engineering — GPA: 3.9/4
University of Southern California (USC) — Aug 2017 – May 2022(Expected)

M.Sc. in Computer Science — GPA: 3.85/4
University of Southern California (USC) — Aug 2017 – Dec 2020 (Expected)
Coursework: Database Systems (CSCI585), Analysis of Algorithms (CSCI570), Deep Learning and its Applications (CSCI 566), Foundations of Artificial Intelligence (CSCI 561), CSCI Special Topics: Computer-Aided Verification (CSCI 699)

M.Sc. in Electrical Engineering — GPA: 4/4
University of Southern California (USC) — Aug 2017 – May 2020
Coursework: VLSI System Design (EE577A), Computer-Aided Design of Digital Systems (EE681), Mathematical Foundations for System Design (EE599), Introduction to Programming Systems Design (CSCI 455)

SKILLS

- **Programming languages:** C/C++/C#, Python, and Assembly programming. **Version Control:** Git.
- **Hardware Languages:** Verilog, VHDL, SystemVerilog, SystemC. **Databases:** SQL, MySQL, Postgres, PostGIS.
- **Tools:** MATLAB, Xilinx Vivado (HLS), Xilinx SDAccel, Cadence and Synopsys tools, Quartus, Keras, TensorFlow, Pytorch, TinkerPop.

HONORS AND AWARDS

- Selected as a recipient of the DAC young fellow poster presentation awards. — July 2020
- **Awarded** DAC Young Fellowship for attending 57th ACM/IEEE Design Automation Conference**.** — July 2020
- **Ranked** the first student among 120 students of Electrical Engineering — 2010 - 2014
- **Ranked** the second team in the Second National Robocup (Soccer 2D Simulation) Competition for Students — March 2008
- **Honorary Admission** to University of Tehran Master program as Exceptional Talent, without entrance exam — 2014
- Awarded Ferdowsi University of Mashhad scholar as **distinguished B.Sc. graduate** of year — 2014

PROJECTS

- **Memory-Efficient FPGA-based CNN Acceleration [Pytorch, Python, Verilog, C/C++, OpenCL]:** — May 2019-Current
  - Developed a Compiler for scheduling and mapping the high-level modeling of CNNs on FPGA.
  - Designed an accelerator architecture and implemented on FPGA.
- **Tool Flow for enabling Processing-In-Memory for Memristive Crossbars [Python, SPICE]:** — May 2019-Current
  - Novel logic synthesis approach with a dedicated mapping strategy tailored on MAGIC crossbars.
  - Significantly improved both the average computational latency (2.12x) and area (1.38x).
- **Deep-learning-based CAD tools [C++, Python, Tensorflow, Verilog]:** — Mar 2018-Current
  - Created a tool for efficiently recognizing functionality of a circuit leveraging deep learning.
  - Proposed a convolutional neural network (CNN)-based circuit representation.
- **Post-synthesis verification of superconductive electronic circuits [C++, Python, SystemVerilog]:** — Jan 2018-Current
  - Presented a novel graph representation of the beyond-CMOS circuit to be utilized in formal methods.
  - Successfully implemented a novel learning-based UVM-compliant verification framework.
- **Design and implementation of neuromorphic circuits [MATLAB, SPICE, Python]:** — Aug 2015-Current
  - developed ultra-low power smart sensor using high-speed NN-based ADC/DAC.
  - Actively working on developing efficient training algorithms and CAD tool to facilitate memristive-based circuit implementation.
- **Approximate Computing [MATLAB, Verilog]:** — Aug 2014-Aug 2015
  - Developed a high-speed yet energy efficient approximate divider; Successfully implemented in hardware.
  - 14x and 300x smaller delay and energy consumption compared to the Radix-2 SRT.

ACADEMIC EXPERIENCE & PROFESSINAL SERVICES

- Closely mentoring 6 graduate students and involve them with the research including functional verification of superconductive electronic circuits, improving the functional coverage utilizing machine learning algorithm, publish results in ISQED'19 and GLSVLSI'19. — Jan 2018- Current
- Teaching Assistant (Electronic II, Computer Architecture) & Verilog Instructor (Computer Architecture laboratory). — Aug 2013- May 2016
- Collaborated in a study group of 15 students and implemented LED Cube using MATLAB and manufacture it, held by IEEE branch of Ferdowsi University of Mashhad. — Summer 2011
- Reviewer of IEEE TNNLS, TCAD, TAS, TCAS II and Access journals. — Jan 2019- Current

SELECETED PUBLICATIONS

- qEC: A Logical Equivalence Checking Framework Targeting SFQ Superconducting Circuits, *ISEC 2019.*
- Deep Learning-Based Circuit Recognition Using Sparse Mapping and Level-Dependent Decaying Sum Circuit Representations, *DATE 2019*.
- OCTAN: An On-Chip Training Algorithm for Memristive Neuromorphic Circuits, *IEEE TCAS I 2020.*
- Inverter-based Memristive Neuromorphic Circuit for Ultra-low-power IoT Smart Applications, *A book chapter published in IET Book on Hardware Architectures for Deep Learning, 2020*.