USC Viterbi School of Engineering

Arash Fayyazi

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EDUCATION

Ph.D. in Electrical Engineering, Minor- Computer Engineering University of Southern California (USC)	GPA: 3.90/4 August 2017 – May 2022 (Expected)
M.Sc. in Computer Science University of Southern California (USC) *Coursework*: Database Systems (CSCI585), Analysis of Algorithms (CSCI570), Deep Learning and its Applications (CSCI 566), Introduction to Programming Systems Design (CSCI 455), Foundations of Artificial Intelligence (CSCI 561), CSCI Special Topics: Computer-Aided Verification (CSCI 699)	GPA: 3.85/4 August 2017 – December 2020 (Expected)
M.Sc. in Electrical Engineering University of Southern California (USC) *Coursework*: Probability for Electrical and Computer Engineering (EE503), VLSI System Design (EE577A), Computer-Aided Design of Digital Systems (EE681), EE Special Topics: Mathematical Foundations for System Design (EE599), Foundations of Artificial Intelligence (CSCI 561), Introduction to Programming Systems (CSCI 455)	GPA: 4/4 August 2017 – May 2020
M.Sc. in Electrical Engineering – Electronics, Minor in Circuits and Systems University of Tehran (UT) *Coursework*: Custom implementation of DSP systems, Advanced Topics in Computer Architecture – Chip Multiprocessors, pre- and post-silicon debugging of digital systems, VLSI System Design	GPA: 4/4 August 2014 – January 2017

SKILLS

- **Programming languages:** C/C++/C#, HTML, Python, Promela, and Assembly programming.
- **Hardware Languages:** Verilog, VHDL, SystemVerilog, SystemC.
- **Tools:** MATLAB, HSPICE, Cadence Virtuoso, NCSim, VCS, UVM, Xilinx ISE Design Suite, Quartus, Proteus, Keil, Code Vision AVR Compiler, Orcad Pspice, GEM5, UPPAL, MiniSAT, SPIN, NuSMV, Keras, TensorFlow, Pytorch, TinkerPop, Visio.
- **Language:** Persian (Native), English (Fluent), Arabic (Intermediate)
- **Version Control:** Git.
- **Databases:** SQL, MySQL, Postgres, PostGIS.

HONORS AND AWARDS

❖ Selected as a recipient of the DAC young fellows poster presentation awards.	July 2020
❖ Awarded DAC Young Fellowship for attending 57th ACM/IEEE Design Automation Conference	July 2020
❖ Awarded Student Travel Support for attending International Superconductive Electronics Conference	July 2019
❖ **Ranked** the third student among 28 students of Electronics Engineering- Major – Circuits and Systems	2014 – 2017
❖ **Ranked** the first student among 40 students of Electronics Engineering	2010 – 2014
❖ **Ranked** the first student among 120 students of Electrical Engineering	2010 - 2014
❖ **Ranked** the 7th in Robocup IranOpen 2008 International Competition in Qazvin, Iran (League: Soccer 2D simulation)	April 2008
❖ **Ranked** the second team in the Second National Robocup (Soccer 2D Simulation) Competition for Students	March 2008
❖ Member of **Exceptional Talents** in Ferdowsi University of Mashhad	2010 – 2014

- **Honorary Admission** to University of Tehran Master program as Exceptional Talent, without national entrance exam 2014
- Awarded Ferdowsi University of Mashhad scholar as **distinguished B.Sc. graduate** of the year 2014

PUBLICATION

Refereed Book Chapters

- **Arash Fayyazi,** Mohammad Ansari, Mehdi Kamal, Ali Afzali-Kusha, Massoud Pedram, "Inverter-based Memristive Neuromorphic Circuit for Ultra-low-power IoT Smart Applications", *IET Book on Hardware Architectures for Deep Learning, ISBN-13: 978-1-78561-768-3, 2020.*

Peer-Reviewed Journals

- Mohammad Ansari, **Arash Fayyazi,** Ali Banagozar, Mohammad Ali Maleki, Mehdi Kamal, Ali Afzali-Kusha, Massoud Pedram, "PHAX: Physical Characteristics Aware Ex-Situ Training Framework for Inverter-Based Memristive Neuromorphic Circuits", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 2017.*
- **Arash Fayyazi**, Mohammad Ansari, Mehdi Kamal, Ali Afzali-Kusha, Massoud Pedram, "An Ultra-Low-Power Memristive Neuromorphic Circuit for Internet of Things Smart Sensors", *IEEE internet of things journal, 2018*.
- Ramy N Tadros, **Arash Fayyazi,** Massoud Pedram, Peter A Beerel, "SystemVerilog modeling of SFQ and AQFP circuits", IEEE Transactions on Applied Superconductivity, 2019.
- Mohammad Ansari, **Arash Fayyazi,** Mehdi Kamal, Ali Afzali-Kusha, Massoud Pedram, "OCTAN: An On-Chip Training Algorithm for Memristive Neuromorphic Circuits", *IEEE Transactions on Circuits and Systems I: Regular Papers (TCAS I)*, 2019.

Refereed Full-Length Conference Proceedings

- Reza Zendegani, Mehdi Kamal, **Arash Fayyazi**, Ali Afzali-Kusha, Saeed Safari, Massoud Pedram, "SEERAD: A high speed yet energy-efficient rounding-based approximate divider". *IEEE Design, Automation & Test in Europe Conference & Exhibition* (*DATE), 2016*.
- Alvin D Wong, Kevin Su, Hang Sun, **Arash Fayyazi**, Massoud Pedram, Shahin Nazarian, "VeriSFQ: A semi-formal verification framework and benchmark for single flux quantum technology", *IEEE 20th International Symposium on Quality Electronic Design (ISQED), 2019.*
- **Arash Fayyazi,** Soheil Shababi, Pierluigi Nuzzo, Shahin Nazarian, Massoud Pedram, "Deep Learning-Based Circuit Recognition Using Sparse Mapping and Level-Dependent Decaying Sum Circuit Representations", *IEEE Design, Automation & Test in Europe Conference & Exhibition* (*DATE), 2019*.
- Karunveer Singh, Rishabh Gupta, Vikram Gupta, **Arash Fayyazi,** Massoud Pedram, Shahin Nazarian, "A Hybrid Framework for Functional Verification using Reinforcement Learning and Deep Learning", *Proceedings of the 2019 on Great Lakes Symposium on VLSI* (*GLSVLSI), 2019.*
- **Arash Fayyazi,** Souvik Kundu, Shahin Nazarian, Peter A Beerel, Massoud Pedram, "CSrram: Area-Efficient Low-Power Ex-Situ Training Framework for Memristive Neuromorphic Circuits Based on Clustered Sparsity", *2019 IEEE Computer Society Annual Symposium on VLSI* (*ISVLSI), 2019.*
- **Arash Fayyazi,** Shahin Nazarian, Massoud Pedram, "qEC: A Logical Equivalence Checking Framework Targeting SFQ Superconducting Circuits", *2019 IEEE International Superconductive Electronics Conference (ISEC), 2019.*
- Shahin Nazarian, **Arash Fayyazi**, Massoud Pedram, "qCG: A Low-Power Multi-Domain SFQ Logic Design and Verification Framework", *2019 IEEE 37th International Conference on Computer Design (ICCD), 2019.*

Refereed full-length Conference Accepted Articles

- **Arash Fayyazi,** Amirhossein Esmaili Dastjerdi, Massoud Pedram, "HIPE-MAGIC: A Technology-Aware Synthesis and Mapping Flow for Highly Parallel Execution of Memristor-Aided LoGIC", *To be appeared in IEEE/ACM International Symposium on Low Power Electronics and Design (ISLPED), 2020.*
- Mahdi Nazemi, Amirhossein Esmaili, Arash Fayyazi, and Massoud Pedram. "SynergicLearning: Neural Network-Based Feature Extraction for Highly-Accurate Hyperdimensional Learning". *To be appeared in IEEE/ACM International Conference on Computer-Aided Design (ICCAD), 2020.*

Preprint Articles

- **Arash Fayyazi**, Souvik Kundu, Shahin Nazarian, Peter A Beerel, Massoud Pedram, "CSrram: Area-Efficient Low-Power Ex-Situ Training Framework for Memristive Neuromorphic Circuits Based on Clustered Sparsity", *arXiv preprint arXiv:1809.03476, 2018.*
- **Arash Fayyazi,** Shahin Nazarian, Massoud Pedram, "Logic Verification of Ultra-Deep Pipelined Beyond-CMOS Technologies", *arXiv preprint arXiv:2005.13735, 2020.*

ACADEMIC EXPERIENCE

- closely mentoring 12 graduate students and two undergrad students and involve them with the research, including functional verification of superconductive electronic circuits, improving the functional coverage utilizing machine learning algorithm, publish results in ISQED'19 and GLSVLSI'19. — January 2018- Current
- Teaching Assistant (Electronic II, Computer Architecture) & Verilog Instructor (Computer Architecture laboratory). — August 2013- May 2016
- Led team of 3 students to participate in the 1st and 2nd national digital design Competition. — March 2014- April 2015
- Collaborate with a team of 5 volunteer students responsible for realizing Digital Designing Lab. — January 2013- May 2013
- Collaborated in a study group of 15 students and implemented LED Cube using MATLAB and manufacture it, held by the IEEE branch of the Ferdowsi University of Mashhad. — Summer 2011
- Research Assistant at the System Power Optimization and Regulation Technology (SPORT LAB): Exploring Energy-efficient computing using beyond-CMOS technology. — August 2017 – present

PROJECTS

- **Memory-Efficient FPGA-based CNN Acceleration [Pytorch, Python, Verilog, C/C++]:** — May 2019- Current
  - Actively working on developing a tool for mapping pruned CNNs on FPGAs efficiently.
  - Developed a Compiler for scheduling and mapping the high-level modeling of CNNs on FPGAs.
  - Designed an accelerator architecture and implemented on FPGA.
- **Tool Flow for enabling Processing-In-Memory for Memristive Crossbars [Python, SPICE]:** — May 2019- Current
  - New logic synthesis approach with a dedicated mapping strategy tailored to MAGIC crossbars.
  - Significantly improved both the average computational latency (2.12x) and area (1.38x).
- **Deep-learning-based CAD tools for design and verification of digital circuits [C++, Python, Tensorflow, Verilog]:** — March 2018- Current
  - Created a tool for efficiently recognizing the functionality of a circuit leveraging deep learning.
  - Proposed a convolutional neural network (CNN)-based circuit representation.

- **Post-synthesis verification of superconductive electronic circuits [C++, Python, SystemVerilog]:** January 2018-Current
  - Presented a novel graph representation of the beyond-CMOS circuit to be utilized in formal methods.
  - Successfully implemented a novel learning-based UVM-compliant verification framework.
- **Design and implementation of neuromorphic circuits [MATLAB, SPICE, Python]:**
  - developed ultra-low-power smart sensor using high-speed NN-based ADC/DAC.
  - Actively working on developing efficient training algorithms and CAD tools to facilitate memristive-based circuit implementation. August 2015-Current
  - **M.Sc project:** Designed and implemented neuromorphic circuits as an analog coprocessor for a digital processing system, developed ultra-low power smart sensor using high-speed ADC/DAC, develop efficient training algorithms and CAD tool to facilitate memristive-based circuit implementation.
- **Approximate Computing [MATLAB, Verilog]:** August 2014-August 2015
  - Developed a high-speed yet energy-efficient approximate divider; Successfully implemented in hardware.
  - 14x and 300x smaller delay and energy consumption compared to the Radix-2 SRT.
- Designed and implemented "Blokus Duo" and "Trax Game" solver on Altera DE2-115 in the 1st and 2nd National Digital System Design Contest of Iran **[Verilog, VHDL, C].** March 2014-April 2015
- Designed and developed a multi-cycle and a pipelined MIPS processor with using On-chip SRAM as Cache, 15-point FFT Engine, Digital FIR Filter, FIFO **[Verilog, VHDL]**. Spring 2012-2015

Services and Memberships

- IEEE Student member.
- Reviewer of IEEE transactions on neural networks and learning systems journal.
- Reviewer of IEEE Access journal.
- Reviewer of IEEE Transactions on Applied Superconductivity.
- Reviewer of Springer CCF Transactions on High Performance Computing.
- Reviewer of IEEE Transactions on Electron Devices.
- Reviewer of IEEE Transactions on Circuits and Systems II: Express Briefs.
- Reviewer of Design Automation Conference (2020).